

# Editorial

## R&D lag threatens Si, compound & nano

This year for CS Mantech, DARPA's John Zolper co-authored on integrated micro systems as the next technology transition. Highlighted is the fact that it is circuit level capability, measured by speed, power and precision that is 'king,' rather than simply device level performance.

The work to achieve this is not insignificant. Vitesse's InP circuit performance achievement (page 34) has not only required device redesign, but a purpose built processing line.

"And as CMOS scaling and integration are considered – systems containing a trillion transistors, dissipating less than 100W (about the complexity of the human brain) the vision is of the integrated microsystem and the 3D circuit – heterogenous integration; volumetric system scaling; VLSI of photonic and optoelectronic components into traditional CMOS circuits."

"Researchers are using MEMS techniques to produce arrays of nano-resonators that can be integrated with other components *in silico*" and "DARPA has launched a major initiative to develop supporting technologies to start the revolution of the integrated Microsystems." Sematech has been quick to add 3D interconnects to its top technical challenges for 2005.

But as the Semiconductor Industry Association reports record sales – a 2004 growth of 28.6% with \$214bn, surpassing the \$204bn of 2000 – an ominous if less publicised problem lurks behind such forecasts. It is that both US and European top researchers report that R&D funds are at an all time low. The suggestion that this

changes if "nanotechnology" can be attached to projects, draws a wry look.

John E. Kelly III, senior VP and group exec of the IBM Technology Group puts it succinctly, with a slant that is as valid for Europe. "State-of-the-art, 300mm fabs with 90nm process technology are coming on line in other parts of the world. No one doubts that the links between R&D and manufacturing are becoming more important, these links are dynamic, and proximity between labs and fabs is also an issue.

Because US semiconductor R&D efforts currently face an annual shortfall of approximately \$1.5bn, Kelly is urging SIA members to bring investments in line to stay current with the CMOS technology roadmap, as well as to extending technology beyond CMOS.

"Public policy must not only encourage R&D activities in the US, but also provide an attractive climate for investing in production capacity in the US," noted Kelly. "Constant innovation is the key to being competitive while paying high wages to our workforce."

If R&D falls by the wayside, there's a deeper worry factor and that's the sector's appeal to the student and the ability of the Universities to gear sufficiently multidisciplinary courses to equip the next work force for the nano, compound and silicon revolutions.

Gail Purvis, Editor




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III-Vs Review is published nine times a year. Periodicals postage is paid at Rahway, NJ 07065. Postmaster send address corrections to: III-Vs Review, 365 Blair Rd, Avenel, NJ 07001.

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Printed by: The Manson Group Ltd, St Albans, UK.  
Journal Number: 02076 ISSN 0961-1290

Colbitre Gloss is manufactured from ECF pulp produced from renewable forest resources. ECF pulp is pulp bleached without using elemental chlorine

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